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Term	Documents
(16 AND 20).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	2
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L23	L20 and l15	22	L23
L22	L20 and l14	96	L22
L21	L20 and l13	185	L21
L20	L19 and (available or ready) near5 execut$6	237	L20
L19	L18 and conditio$3 near4 branch$3	428	L19
L18	l12 and (sequen$5 or order) near6 (instruction$1 or execut$5 or process$3)	626	L18
DB=PGPB,USPT; PLUR=YES; OP=OR			
L17	l12 and L13	457	L17
L16	(711/123,125)![CCLS]	426	L16
L15	(711/123-221)![CCLS]	18080	L15
L14	(712/23,215,219,234,245)[CCLS]	1917	L14

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L13	(712/2-300)[CCLS]	10713	L13
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L12	L11 and (identif$9 or id$1) near6 (resourc$3 or element$1 or unit$1 or thread$3 or instruction$1 or memor$4 or buffer$1 or stor$4 or register$1)	640	L12
L11	L10 and (concurrent$2 or simultaneous$3 or parallel$4) near5 issu$6	845	L11
L10	instruction$1 near3 buffer$5	10861	L10
DB=PGPB,USPT; PLUR=YES; OP=OR			
L9	L6 or l4	12	L9
DB=PGPB,USPT,USOC,EPAB,JPAB; PLUR=YES; OP=OR			
L8	L6 or l4	12	L8
DB=USPT; PLUR=YES; OP=OR			
L7	L6 or l4	6	L7
L6	5539911.pn. or 5689720.pn. or 6092181.pn. or 6038654.pn. or 6256720.pn. 6647485.pn.	6	L6
DB=PGPB; PLUR=YES; OP=OR			
L5	5539911.pn. or 5689720.pn. or 6092181.pn. or 6038654.pn. or 6256720.pn. 6647485.pn.	0	L5
L4	20030079113.pn. or 20030070060.pn. or 20030056087.pn. or 20040054872.pn. or 20040093485.pn. or 20040093482.pn.	6	L4
L3	20030056086.pn.	1	L3
DB=USPT; PLUR=YES; OP=OR			
L2	20030056086.pn.	0	L2
L1	20030056086	0	L1

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1 **Optimization of instruction fetch mechanisms for high issue rates**
Conte, T.M.; Menezes, K.N.; Mills, P.M.; Patel, B.A.;
Computer Architecture, 1995. Proceedings. 22nd Annual International Sympos on , 22-24 June 1995
Pages:333 - 344

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2 **The Gmicro/500 superscalar microprocessor with branch buffers**
Uchiyama, K.; Arakawa, F.; Narita, S.; Aoki, H.; Kawasaki, I.; Matsui, S.; Yamamoto, M.; Nakagawa, N.; Kudo, I.;
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Wallace, S.; Bagherzadeh, N.;
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4 **Advanced performance features of the 64-bit PA-8000**
Hunt, D.;
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Ikumi, N.; Tanaka, S.; Sawada, K.; Nagamatsu, M.; Kondo, Y.; Takayanagi, T Minagawa, K.; Akiba, H.; Miyamoto, K.; Hiruta, Y.; Hsu, P.; Rodman, P.; Brat Man Kit Tang; Nofal, M.; Joshi, C.; Scanlon, J.;
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8 **Integrating a misprediction recovery cache (MRC) into a superscala pipeline**
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16 **Isolating short-lived operands for energy reduction**
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